OPTIMIZATION OF DISTRIBUTED MONOLITHIC GaAs AMPLIFIERS USING AN ANALYTICAL/GRAPHICAL TECHNIQUE

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ABSTRACT

An analytical/graphical procedure provides a close approximation to the optimum design of a distibuted monolithic GaAs amplifier, given specific gain and 1-dB bandwidth requirements. The technique gives the optimum number of stages, the FET dimensions and the values of the lumped inductors used to realize the artifical transmission lines.

INTRODUCTION

Conventional design approaches for distributed monolithic GaAs amplifiers typically involve a detailed computer simulation, followed by numerical optimization [1]; the derivation of approximate formulas, again followed by optimization [2, 3]; or by graphical techniques aimed at achieving the maximum possible gain-bandwidth product for a given transistor design [4,5]. In contrast, this paper presents a simple non-computer procedure which provides not only the optimum values of the lumped-element circuit components but also the optimum design of the FETs themselves.

THEORY

The distributed amplifier circuit of Fig.1 uses lumped inductors and is similar to that in [4]. Fig.2 shows the small-signal FET model [6]. Here it is assumed that the parasitics R_g, R_s and R_d are negligible. We also assume that the FETs are unilateral, i.e. that C_{ds} is negligible, so that the gate and drain lines can be treated separately. The resulting equivalent circuit is shown in Fig.3. Gate- and drain-line losses are due to R_i and R_{ds} respectively.

If the gate and drain lines have matched terminations, and are constrained by making

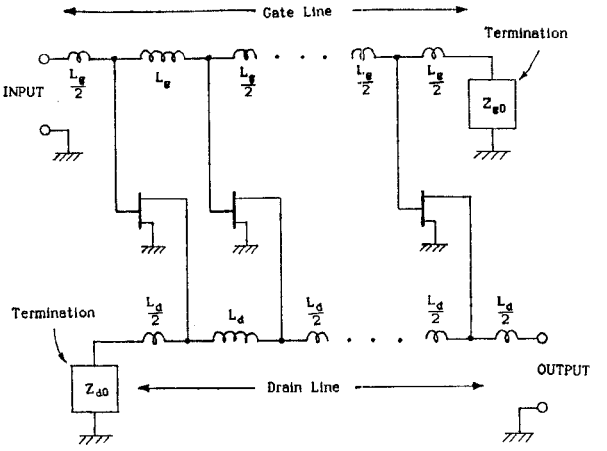

Fig.1 Basic distributed amplifier.

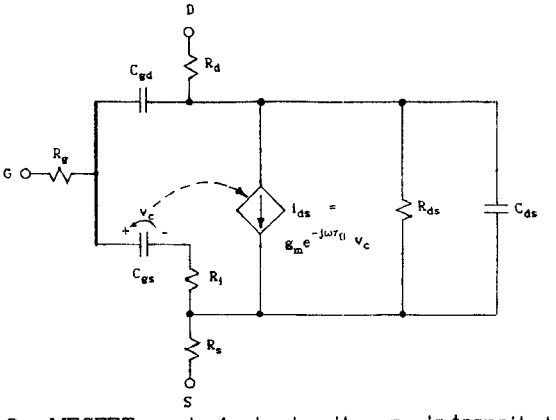

Fig.2 MESFET equivalent circuit. τ_0 is transit time.

$$L_g = L_d = L \quad (1)$$

and

$$C_{gs} = C_{ds} + C_p = C \quad (2)$$

(where C_p is an additional shunt capacitance), then the lines have equal characteristic impedances

$$Z_{g0} = Z_{d0} = \sqrt{\frac{L}{C}} = Z_0 , \quad (3)$$

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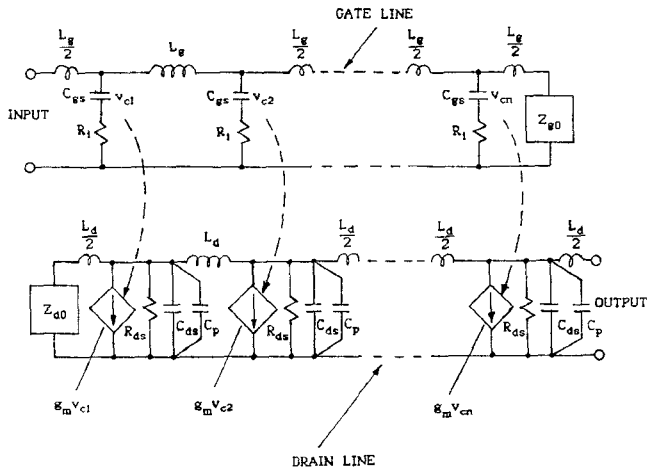

Fig.3 Equivalent distributed MESFET amplifier circuit, showing the artificial gate and drain lines.

as well as equal cutoff frequencies

$$\frac{2}{\sqrt{LC}} = \omega_c \,. \tag{4}$$

With these constraints the normalized voltage gain is, as in [4],

$$A_N(\Omega) = \frac{A(\Omega)}{A_0} = \frac{\sinh(b/n)\,\sinh(\xi)\,e^{b}\,e^{-\zeta}}{\sinh(b)\,\sinh(\xi/n)\sqrt{1-\Omega^2}\sqrt{1+(2a\Omega/n)^2}} \tag{5}$$

where

$$A_0 = \frac{g_m Z_0\, e^{-b}\sinh(b)}{2\,\sinh(b/n)} \tag{6}$$

is the low-frequency voltage gain,

$$\Omega = \frac{\omega}{\omega_c} \tag{7}$$

is the normalized frequency, and the remaining quantities are

$$a = n\left(\frac{R_1}{Z_{g0}}\right), \tag{8}$$

$$b = \frac{n}{4}\left(\frac{Z_{d0}}{R_{ds}}\right), \tag{9}$$

$$\xi = P-Q, \tag{10}$$

$$\zeta = P+Q, \tag{11}$$

$$P = \frac{b}{\sqrt{1-\Omega^2}}, \tag{12}$$

$$Q = \frac{a\Omega^2}{\sqrt{1-[1-(2a/n)^2]\Omega^2}}\,. \tag{13}$$

We next define gate-width-independent parameters characterizing the FET fabrication process:

$$k_{gm} = g_m/W, \tag{14}$$

$$k_c = C_{gs}/W, \tag{15}$$

$$k_{R1} = R_1 W, \tag{16}$$

$$k_{Rds} = R_{ds} W, \tag{17}$$

where W is the FET gate width.

Because of (3), a simple relation between a, b and n can be found [7] from (8), (9), (16) and (17):

$$\boxed{ab = \frac{n^2}{k_n}} \tag{18}$$

where

$$k_n = 4\,\frac{k_{Rds}}{k_{R1}}\,. \tag{19}$$

A simple relation can also be found between a, b and W. From (8), (9), (16) and (17):

$$W = \frac{2}{Z_0}\sqrt{\frac{b}{a}\,k_{Rds}\,k_{R1}}\,. \tag{20}$$

Eqn.(5) is a function of a, b, n and Ω. To reduce the number of variables to three, we replace Ω by Ω_{1dB}, the normalized frequency at which A_N drops by 1 dB. Then $\Omega_{1dB}(a, b, n)$ is the numerical solution of (5) with A_N set equal to 0.8193 and Ω replaced by Ω_{1dB}. The unnormalized 1-dB roll-off frequency is

$$\omega_{1dB} = \Omega_{1dB}(a, b, n)\,.\,\omega_c\,. \tag{21}$$

To remove ω_c from consideration, we use (3), (4), (15) and (22) to obtain

$$\omega_c = \sqrt{\frac{a}{b}}\,\frac{1}{k_c\sqrt{k_{Rds}\,k_{R1}}}\,. \tag{22}$$

Eqn.(21) can now be written in the normalized form

$$\boxed{\overline{\omega_{1dB}} = \sqrt{\frac{a}{b}}\,\Omega_{1dB}(a, b, n)}\,, \tag{23}$$

where

$$\overline{\omega_{1dB}} \triangleq \omega_{1dB}\,k_c\,\sqrt{k_{Rds}\,k_{R1}}\,. \tag{24}$$

Equations (18) and (23) are plotted on the (a, b)-plane in Figs. 4(a)-(c) for n = 3, 4 and 5.

To remove g_m and Z_0 from consideration, we define the "process-independent normalized low-frequency gain" $\overline{A_0}$ by dividing (6) by $g_m Z_0$ and using (14) and (20):

$$\boxed{\overline{A_0}(a,b,n) = \sqrt{\frac{b}{a}}\,\frac{e^{-b}\sinh(b)}{\sinh(b/n)}}\,, \tag{25}$$

where

$$\overline{A_0} \triangleq \frac{A_0}{k_{gm}\sqrt{k_{R1}k_{Rds}}}\,. \tag{26}$$

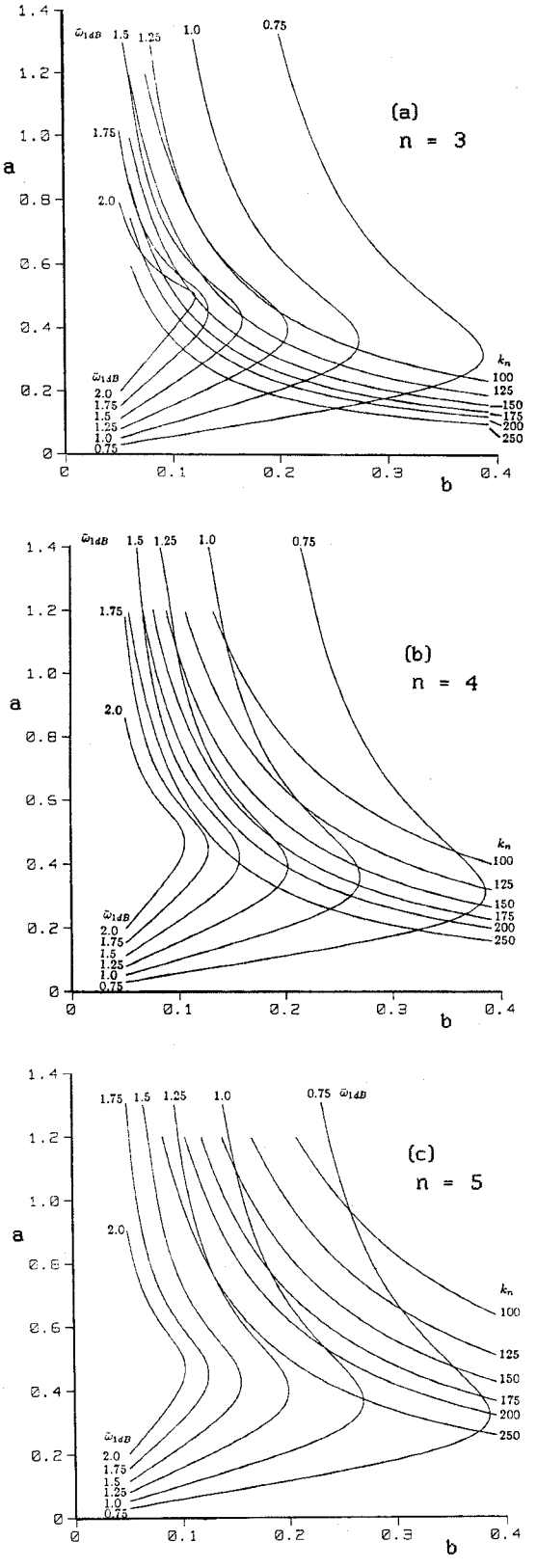

Fig.4 Graphical optimization charts for (a) n = 3, (b) n = 4, (c) n = 5.

DESIGN PROCEDURE

The optimum design point on the (a, b)-plane for a given distributed amplifier can be obtained from the plots of Fig.4. Once this point has been determined for a given FET process and desired 1-dB roll-off point, the following design parameters can be immediately calculated:

- the optimum number of stages n,
- the optimum inductor values L for the lines,
- the optimum FET gate width W, (and hence the intrinsic parameters g_m, C_{gs}, R_i and R_{ds}),
- the low-frequency gain A_0,

such that the gain is maximized across the band of operation.

A suitable procedure is the following.

(a) Obtain the width-independent parameters according to (14)-(17).
(b) Find $\bar{\omega}_{1dB}$ from (24) using (a) and the desired ω_{1dB}.
(c) Calculate k_n from (19).
(d) Starting with n=4, locate the appropriate curves of constant $\bar{\omega}_{1dB}$ and k_n in Fig.4(b) and their point of intersection. If there are two such points, take the one nearest the b-axis. If there is no intersection, no solution exists for this value of n.
(e) From (25), calculate $\bar{A}_0$.
(f) Repeat steps (d) and (e) for n=3 and n=5, using Figs. 4(a) and 4(c). If values of n exceeding 5 are needed, use the curves for n=5, but with k_n multiplied by $n^2/25$.
(g) Hence find values of a, b and n which maximize $\bar{A}_0$. Then A_0 can be calculated from (26), ω_c from (22), and L from (3) and (4), (i.e. $L = 2Z_0/\omega_c$). Z_0 is fixed by external requirements and is normally 50 Ω.
(h) Use the optimum values of a and b to calculate W from (20).
(i) Verify that the approximations implicit in (14)-(17) are still valid. If not, repeat (a) to (h) using revised width-independent FET parameters which are valid for the determined value of W.

EXAMPLE OF OPTIMIZATION

Using FET parameters and ω_{1dB} as given by Beyer et al.[4] (they take W = 300 μm, f_{1dB} = 16.52 GHz):

g_m = 0.04 S
C_{gs} = 0.27 pF
C = C_{ds} + C_p = 0.27 pF
R_{ds} = 300 Ω
R_i = 7 Ω,

execution of the procedure of the previous section results in Table 1. This shows that the maximum value of A_0 is obtained for n = 4. A voltage gain of 3.77 (power gain = 11.5 dB) is achieved using FETs of 339 μm gate-width.

TABLE 1
Graphically-Determined Distributed Amplifier Parameters

n =	3	4	4 (Ref[4])	5
a	0.29	0.49	(0.56)	1.62
b	0.18	0.19	(0.17)	0.09
$\overline{A_0}$	1.98	2.06	(1.87)	1.07
A_0	3.62	3.77	(3.27)	1.96
W (μm)	431	339	(300)	128
Ω_{1dB}	0.77	0.81	(0.70)	0.42
f_c (GHz)	16.5	21.0	(23.6)	55.5
L (nH)	0.96	0.76	(0.67)	0.29
g_m (mS)	57	45	(40)	17
R_i (Ω)	4.9	6.2	(7.0)	16.4
C_{gs} (pF)	0.39	0.31	(0.27)	0.12
R_{ds} (Ω)	209	265	(300)	703

COMPARISON WITH OTHER APPROACHES

Fig.5 shows the frequency response of the 4-stage distributed amplifier optimized by the present method. Also shown is the response of the same amplifier as analyzed by SUPER COMPACT [8]: here the optimum W is 350 μm. The disagreement below ~7 GHz is due to the slight frequency-dependence of the drain-line impedance. The non-optimized result of Beyer et al. [4] is included for comparison.

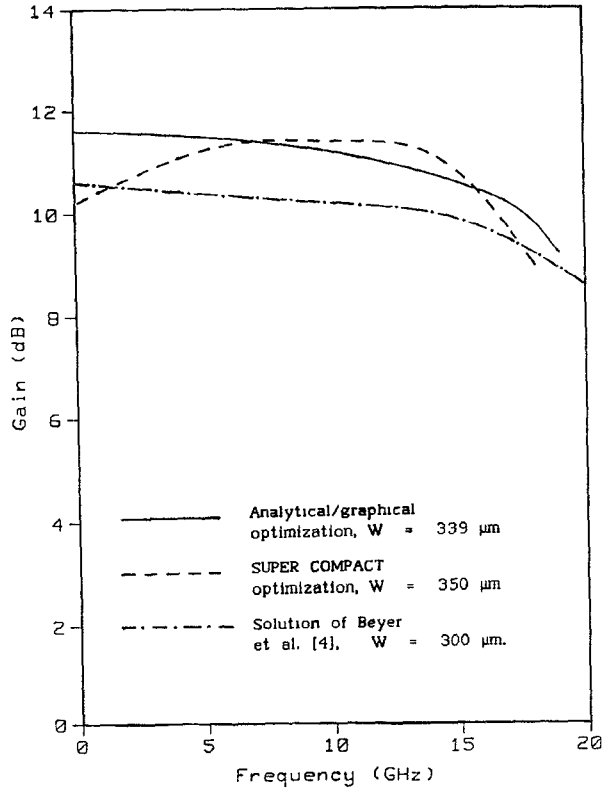

Fig.5 Comparison of frequency responses obtained by the present method, by computer optimization, and by Beyer et al. [4].

CONCLUSIONS

A novel analytical/graphical approach to the optimization of distributed GaAs MESFET amplifiers has been described. Even though a computer is not required, the results obtained compare favourably with those resulting from exhaustive simulations and optimization using conventional numerical techniques.

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